

CLAIMS:

What is claimed is:

1. An apparatus comprising:
a host controller to generate a transaction schedule, the transaction schedule including a plurality of transactions, the plurality of transactions are stored in a plurality of data structures, each of the plurality of data structures contain one of initialized transactions and initialized and non-initialized transactions and the plurality of data structures are isochronous transaction descriptors (iTDs)
wherein the host controller executes the transactions that are initialized and the plurality of data structures each contain a pointer to a next initialized transaction.
2. The apparatus of claim 1, further comprising a host controller driver coupled to the host controller.
3. The apparatus of claim 1, wherein the iTDs are daisy chained into a single classic frame.
4. The apparatus of claim 1, wherein various physical buffer alignments are produced in the transaction schedule.
5. The apparatus of claim 1, wherein the host controller generates a stream of buffers that begin in a middle of a classic frame.
6. The apparatus of claim 1, wherein the host controller generates a plurality of buffers that are variably sized.
7. A method comprising:
determining a starting micro-frame;
receiving buffer data;
creating at least one isochronous transaction descriptor (iTD) based on the starting micro-frame and buffer data;
inserting the at least one iTD into a frame list,

wherein the at least one iTD is contains one of initialized transactions and initialized and non-initialized transactions and the at least one iTD is daisy chained with at least one other iTD into at least one buffer and inserted into a single classic frame.

8. The method of claim 7, further comprising:
initializing an offset and a length; and
initializing a buffer pointer.

9. The method of claim 7, wherein various physical buffer alignments are produced by daisy chaining.

10. The method of claim 7, wherein a stream of buffers that begin in a middle of a classic frame are supported.

11. The method of claim 7, wherein buffers that are variably sized are supported.

12. An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

determining a starting micro-frame;

receiving buffer data;

creating at least one isochronous transaction descriptor (iTD) based on the starting micro-frame and buffer data;

inserting the at least one iTD into a frame list,

wherein the at least one iTD is contains one of initialized transactions and initialized and non-initialized transactions and the at least one iTD is daisy chained with at least one other iTD into at least one buffer and inserted into a single classic frame.

13. The apparatus of claim 12, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

initializing an offset and a length; and

initializing a buffer pointer.

14. The apparatus of claim 12, wherein various physical buffer alignments are produced by daisy chaining.

15. The apparatus of claim 12, wherein a stream of buffers that begin in a middle of a classic frame are supported.

16. The apparatus of claim 12, wherein buffers that are variably sized are supported.

17. A system comprising:
a host controller coupled to a bus, the host controller generates a transaction schedule, the transaction schedule including a plurality of transactions, the plurality of transactions are stored in a plurality of data structures, each of the plurality of data structures contain one of a plurality of initialized transactions, and a plurality of initialized and non-initialized transactions; and
a device coupled to the bus,
wherein the host controller executes the transactions that are initialized and the plurality of data structures each contain a pointer to a next initialized transaction and the plurality of data structures are isochronous transaction descriptors (iTDS).

18. The system of claim 17, further including a host controller driver coupled to the host controller, wherein the bus is a universal serial bus (USB).

19. The system of claim 17, wherein the iTDS are daisy chained into a single classic frame.

20. The system of claim 17, wherein various physical buffer alignments are produced in the transaction schedule.

21. The system of claim 17, wherein the host controller generates a stream of buffers that begin in a middle of a classic frame.

22. The system of claim 17, wherein the host controller generates a plurality of buffers that are variably sized.